

SOFT DECISION BASED TRIPLE-CONCATENATED FEC FOR 100 GB/S SUBMARINE CABLE SYSTEMS

Kiyoshi Onohara, Kazuo Kubo, Yoshikuni Miyata, Hideo Yoshida, Takashi Mizuochi
(Mitsubishi Electric Corporation)

Email: <Onohara.Kiyoshi@eb.MitsubishiElectric.co.jp>

Mitsubishi Electric Corporation, 5-1-1 Ofuna, Kamakura, Kanagawa, 247-8501, Japan

Abstract: We propose a novel soft decision based triple-concatenated FEC. Simulation shows that an NCG of 10.8 dB is obtained by a soft-decision LDPC code concatenated with the enhanced FEC listed in ITU-T G.975.1. A practical implementation of soft decision based FEC for 100 Gb/s submarine cable systems is discussed.

1. INTRODUCTION

New network services employing 40GbE and 100GbE are beginning to drive the submarine cable market and to accelerate its next business cycle. To satisfy the demand for capacity, a digital signal processing based coherent technology, e.g. dual-polarization quadrature-phase-shift keying (DP-QPSK), has begun to be considered for transmitting 100 Gb/s over transoceanic distances [1]. Compared with 10 Gb/s optical transmission, we require 10 dB higher optical signal-to-noise ratio (OSNR) for 100 Gb/s transmission. No matter how well DP-QPSK performs, the OSNR it requires is at best only 6 dB lower than that for on-off keying (OOK). Therefore, at least 4 dB higher OSNR than that for 10 Gb/s OOK is essential for 100 Gb/s DP-QPSK, increasing the demand for powerful forward error correction (FEC) to improve the OSNR capability.

Recently, we reported a real time 32 Gb/s demonstration of the concatenation of a soft decision based low-density parity-check (LDPC) code with a Reed-Solomon (RS) code in a high speed field programmable gate array (FPGA) prototype aimed at showing the feasibility of 3rd generation FEC for 100 Gb/s class optical communications [2]. It was shown that a net coding gain (NCG) of 9.9 dB at a post-FEC bit error ratio (BER) of 10^{-15} can

be expected with 2-bit soft decision and sixteen-fold iterative decoding. An RS(992,956) outer code is effective in cleaning up the undesired error floor generated by the LDPC(9216,7936) inner code. This forward-looking approach was, however, not fully integrated, with only 10 Gb/s of the channel integrated for soft-decision decoding. Therefore further improvement is desirable to achieve 100 Gb/s throughput.

In this paper, we propose a novel soft decision based triple-concatenated FEC. Its features are: (1) the concatenation with a soft decision based LDPC code of an enhanced FEC (EFEC) comprising a concatenated pair of hard decision based block codes having 6.7% redundancy; (2) approximately 20% overall redundancy compliant with optical internetworking forum (OIF) standards, resulting in a transmission rate of 125 Gb/s; (3) an NCG of 10.8 dB at an output BER of 10^{-15} , which is at least 2 dB better than that of hard decision based EFEC for 40 Gb/s [3]; and (4) an optical transport unit – level 4 (OTU4V) frame format compliant with ITU-T G.709 [4]. In addition, we discuss the practical implementation of a soft decision based FEC for 100G transport systems.

2. TRIPLE-CONCATENATED SOFT DECISION FEC SCHEME FOR 100 GB/S TRANSPORT SYSTEMS

Fig. 1 shows the performance objectives of our proposed triple-concatenated soft decision FEC for 100 Gb/s systems. To achieve an NCG of more than 10 dB, we must optimize the combination of concatenated codes for the higher BER region. In a conventional combination, the residual error rate after decoding at the inner code is normally less than 10^{-6} to enable full correction by an outer code such as an RS(255, 239) FEC compliant with ITU-T G.975 (Fig. 1(a) & (b)). Our approach is to apply an LDPC code as the inner code for the higher BER region ($\text{BER} > 10^{-3}$) and a powerful concatenated code set as the outer code for the lower BER region ($\text{BER} < 10^{-3}$), as shown in Fig. 1(c) & (d). LDPC codes show good error correction performance for high BERs from 10^{-2} to 10^{-3} . If the LDPC code is aimed at good error correction performance in this higher BER region, an increase in the residual BER floor is inevitable (Fig. 1(c)). In order to maintain the system performance, we combine a set of powerful concatenated outer codes with the LDPC code (Fig. 1(d)).

The FEC design is based on an irregular LDPC code with codeword and information lengths of 4608 and 4080 respectively, and having 12.9% redundancy. The error correction performance of the LDPC(4608, 4080) alone and the concatenated LDPC(4608,

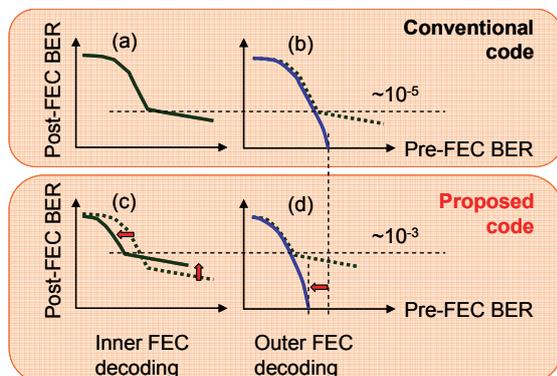


Figure 1: Performance of proposed triple-concatenated soft decision FEC

4080) + EFEC were evaluated by Monte Carlo simulation. For the EFEC, BCH(3860,3824) + BCH(2040,1930) or RS(1023,1007) + BCH(2047,1952), both listed in ITU-T G.975.1 [5], were selected. Fig. 2 shows the simulated pre-FEC Q vs. post-FEC BER. The number of soft decision bits and the number of iterations of the LDPC code were set to three and sixteen respectively. In the case of the LDPC code alone, an undesired error-floor appears clearly at a post-FEC BER of around 10^{-5} . On the contrary, we see no error floor when the LDPC code is concatenated with the EFEC, at least down to a post-FEC BER of 10^{-10} . The frame error ratio (FER) of the LDPC code alone in the water-fall region is about 10^{-1} , but the frequency of less than ten remaining error bits in one codeword is about 60% and that of more than one hundred remaining error bits is zero, so all the residual errors can be cleaned up. Consequently, we expect that the proposed concatenated codes can achieve a Q-limit of 6.4 dB and an NCG of 10.8 dB at a post-FEC BER of 10^{-15} , which is 4.6 dB better than the standard RS(255,239) FEC.

3. CIRCUIT IMPLEMENTATION

As stated in Section 1, we have developed FPGA emulator boards for the concatenation of a soft decision based LDPC code with an RS code, where eight 90 nm process FPGAs were used for the four-iteration LDPC decoding. If we implement the triple-concatenated soft

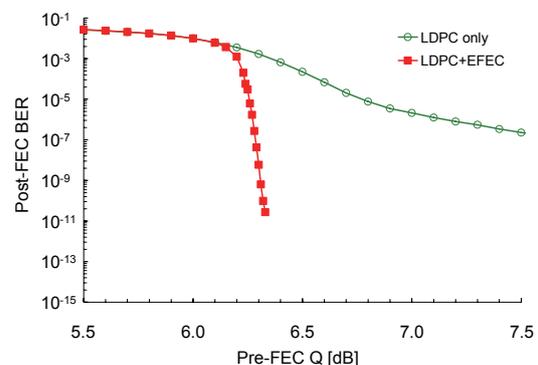


Figure 2: Simulation results for proposed triple-concatenated soft decision FEC

decision FEC with sixteen iterations discussed in Section 2 for 100 Gb/s throughput using the same architecture, over 500 million gates will be needed. This cannot be expected to be feasible, so we consider several approaches to address the circuit implementation issue.

One approach is to partition the large scale integration (LSI), such that the LDPC encoder/decoder is implemented in the digital coherent transceiver, while the EFEC encoder/decoder is implemented in the OTU4 framer. Fig. 3 shows an example of a block diagram of an optical transceiver with digital coherent technology and triple-concatenated soft decision FEC. The optical transceiver consists of an OTU4 framer with a hard decision EFEC encoder/decoder for the outer codes and a digital signal processor (DSP) with a soft decision LDPC encoder/decoder for the inner code.

A second approach is to shorten the length of the LDPC code. A longer LDPC code can achieve better error-correction performance. However, connecting the computation circuits and memories is very difficult because the Tanner graph defined by the parity-check matrix of the LDPC code becomes more complex, and the memories become larger, resulting in a tremendously large circuit. The length of the LDPC code in the proposed triple-concatenated FEC is half that of the LDPC code we demonstrated previously.

A third approach is to improve the error-

correction algorithm. It is known that the best performance for LDPC codes is obtained using the Shuffled Belief Propagation (BP) algorithm [6]. However, the Shuffled BP algorithm requires an enormous circuit. To reduce the circuit complexity, an Offset BP-based algorithm was proposed [7], but its error-correction performance is not so good. So, we designed a novel decoding algorithm, a variable offset BP-based algorithm, so as to minimize the circuit complexity without sacrificing error correction performance [8]. This algorithm stems from the offset BP-based algorithm.

In addition to the above approaches, state-of-the-art LSI processes such as 45 nm promise feasible circuit implementation of the proposed powerful FEC for 100 Gb/s.

Looking again at Fig. 3, we have to note that inter-lane skew at the receiver, which is caused by polarization mode dispersion (PMD), chromatic dispersion in transmission and nonlinear phase noise along the optical fiber, affects the LDPC decoding performance. In order to address this issue, multi-lane distribution (MLD) is also implemented in the DSP to handle the skews and the lane switching. There are four lanes because the DP-QPSK signal format has four channels due to its dual polarized, in-phase and quadrature-phase components. An FEC frame is constructed for each lane individually. Separating the FEC frames prevents the skews and the order of the lanes from affecting the performance of the LDPC codes. This

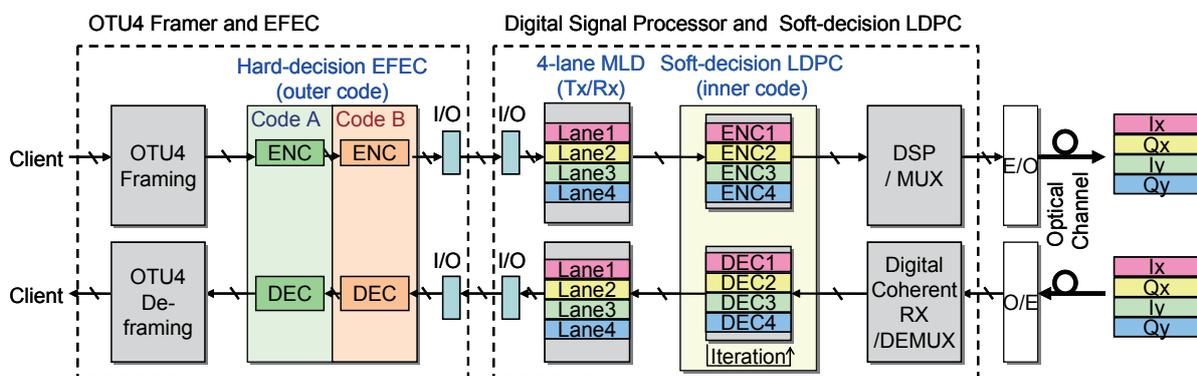


Figure 3: Block diagram of optical transceiver for 100G submarine cable systems

shows that adopting an FEC frame separation scheme along with multiple transmission lanes can overcome the undesirable impairment caused by incomplete data recovery in the DSP.

4. IMPACT ON NEXT GEN SLTE

A digital coherent transceiver with this powerful FEC pushes a submarine line terminal equipment (SLTE) with 100 Gb/s interfaces towards fruition. What is more, a range of interfaces such as 2×40 Gb/s and 10×10 Gb/s could be implemented, enabling submarine carriers to offer diversified and advanced services. In addition, we gain relief from the need for dispersion compensation fibers by implementing a dispersion compensator in the DSP. In particular, pure-silica fiber can be installed when constructing new cable systems, resulting in reduced capital expenditure. Furthermore, this powerful FEC enables us to migrate from existing 40 Gb/s long-haul systems to 100 Gb/s DP-QPSK systems. For example, when compared to 40 Gb/s differential quadrature phase shift keying (DQPSK) and differential phase shift keying (DPSK), 100 Gb/s DP-QPSK requires respectively 1.6 dB and 2.7 dB higher OSNR at a BER of 1.1×10^{-3} . Even if an existing 40 Gb/s DPSK system uses strong EFEC with an NCG of over 8.0 dB, which yields a BER below 10^{-15} , we can migrate it to 100 Gb/s without any replacement of the optical repeaters in the submarine cable thanks to the 10.8 dB NCG of the proposed FEC. We believe that the proposed soft decision based triple-concatenated FEC will have a large positive impact on future submarine cable systems in the 100G era.

5. CONCLUSIONS

We have proposed a triple-concatenated FEC to achieve an NCG of more than 10 dB. The practical implementation of soft decision based FEC for 100G submarine cable systems has been discussed. We believe that the proposed

concept of soft decision based triple-concatenated FEC and this implementation scheme will have a large positive impact on next generation 100G submarine cable systems.

This work was in part supported by the "Digital Coherent Optical Transceiver Technologies" project of the Ministry of Internal Affairs and Communications (MIC) of Japan.

6. REFERENCES

- [1] K. Roberts, M. O'Sullivan, K. Wu, H. Sun, A. Awadalla, D. J. Krause, and C. Laperle, "Performance of dual-polarization QPSK for optical transport systems," *IEEE J. Lightwave Technol.*, vol. 27, no. 16, pp. 3546-3559, (2009).
- [2] T. Mizuochoi, Y. Konishi, Y. Miyata, T. Inoue, K. Onohara, S. Kametani, T. Sugihara, K. Kubo, H. Yoshida, T. Kobayashi, and T. Ichikawa, "Experimental demonstration of concatenated LDPC and RS codes by FPGAs emulation," *Photon. Technol. Lett.*, vol. 21, no. 18, pp. 1302-1304 (2009).
- [3] Y. Kisaka, S. Aisawa, M. Tomizawa, Y. Miyamoto, K. Terada, N. Iwasaki, A. Sano, H. Masuda, and M. Koga, "Fully transparent multiplexing and transport of 10GbE-LANPHY signals in 44.6-Gbit/s-based RZ-DQPSK WDM transmission," in *Proc. OFC/NFOEC2007, OThL1, Anaheim, CA* (2007).
- [4] Y. Miyata, Kazuo Kubo, H. Yoshida, and T. Mizuochoi, "Proposal for frame structure of optical channel transport unit employing LDPC codes for 100 Gb/s FEC," in *Proc. OFC/NFOEC2009, NThB2, San Diego CA* (2009).
- [5] ITU-T Recommendation G.975.1, "Forward error correction for high bit-rate DWDM submarine systems" (2004).
- [6] J. Zhang and Marc P. C. Fossorier, "Shuffled iterating decoding," *IEEE Trans. Commun.*, vol. 53, no. 2, pp. 209-213 (2005).
- [7] J. Chen, A. Dholakia, E. Eleftheriou, M. P. C. Fossorier, and X. Hu, "Reduced-complexity decoding of LDPC codes," *IEEE Trans. Commun.*, vol. 53, no. 8, pp. 1288-1299 (2005).
- [8] Y. Miyata, K. Sugihara, W. Matsumoto, K. Onohara, T. Sugihara, K. Kazuo, H. Yoshida, and T. Mizuochoi, "A triple-concatenated FEC using soft-decision decoding for 100 Gb/s optical transmission," in *Proc. OFC/NFOEC2010, OThL3, San Diego CA* (2010).