EXPERIMENTAL DEMONSTRATION OF TRIPLE-CONCATENATED FEC FOR DIGITAL COHERENT SYSTEMS AND FUTURE FEC TECHNOLOGY

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Abstract: Triple-concatenated forward error correction, realised by concatenating a low-density parity-check (LDPC) code and unequal error protection (UEP) BCH product codes, has been demonstrated experimentally. With a 3-bit soft-decision LDPC code embedded in the coherent DSP and the UEP-BCH codes embedded in the 100 Gb/s Optical Transport Network (OTN) framer, a net coding gain (NCG) of 11.0 dB was achieved with 20.5% redundancy. For the next generation of FEC, we propose to concatenate a spatially-coupled type irregular LDPC with BCH codes. Numerical simulations indicate an NCG of 12.0 dB at a BER of 10^{-15}. It is anticipated that this new FEC will drive increases in the capacity of future submarine cable systems at 100 Gb/s and beyond.

1 INTRODUCTION

Fuelled by the popularity of new high-bandwidth data services such as online storage and video sharing services, telecommunications infrastructure has kept on expanding. This has driven industry-wide efforts to develop the components and systems required to upgrade networks to a 100 Gb/s line rate. In particular, the combination of coherent technology and soft-decision forward error correction (SD-FEC) is accelerating the growth of submarine cable transmission capacity by enabling the introduction of polarisation multiplexed multilevel modulation.

Fig. 1 plots the progress in FECs for optical communication systems over the last twenty-five years. The vertical axis shows the product of linear NCG, defined in terms of a post-FEC BER of 10^{-15}, and bit rate in Gb/s. A clear trend can be seen in that an improvement of 1.4 times has been achieved every year. We started to develop SD-FECs at the end of the 1990s, and demonstrated an experimental Turbo product code at 10 Gb/s for the first time in 2003 [1]. Since then, we have been asserting their importance because of their effectiveness in improving transmission capacity. In 2009, we proposed a triple-concatenated FEC for use with a 100G coherent DSP, with a pair of concatenated hard-decision FECs (HD-FEC) further concatenated with an SD based LDPC code [2]. R&D activities for SD-FECs have accelerated since then [e.g. 3, 4], and SD-FEC is now becoming common in coherent DSPs.

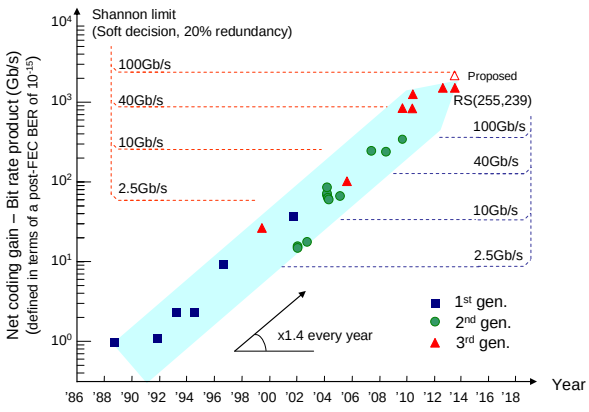

Figure 1: Progress in FECs for optical communication systems.

In this paper, we report the real-time demonstration of a triple-concatenated FEC at a speed of 100 Gb/s, with the soft-decision-based LDPC code embedded in a coherent DSP [5] and the UEP-BCH codes [6] embedded in a 100 Gb/s OTN framer. The UEP is defined such that there are specific bits in the information sequence which are better protected against a large number of errors than other bits. By using UEP-BCH as the outer code, the correction capability can be improved over enhanced FEC compliant with ITU-T G.975.1. In addition, as a next generation FEC, we propose a spatially-coupled type irregular LDPC code. Numerical simulations indicate an NCG of 12.0 dB at a BER of 10^{-15}. The resulting product of NCG and bit rate is indicated by the unfilled triangle in Fig. 1. The future of SD-FEC in submarine cable systems is also discussed.

2 TRIPLE-CONCATENATED FEC

To evaluate the triple-concatenated FEC in real-time operation, we constructed an experimental setup which was fully compliant with the multiplexing and mapping scheme of ITU-T G.709, as shown in Fig. 2. A pseudorandom binary sequence (PRBS) test signal at 103.125 Gb/s is input to the OTU4 framer. Inside the OTU4 framer, a UEP-BCH encoder calculates 7% redundant parity for the OTU4 signal, and an OTU4-framed signal at 111.81 Gb/s is generated. The subsequent gear box, which is a data rate changer using idle bits and high-speed memories, generates a container for the OTU4V frame at a rate of 127.16 Gb/s, and is followed by an LDPC encoder. The LDPC encoder calculates 13% redundant parity, and an OTU4V-framed signal at 127.16 Gb/s is generated. The parallelised OTU4V-framed signal is multiplexed into a serial signal in the multiplexer (MUX). This is then modulated in optical dual polarised quadrature phase shift keying (DP-QPSK) format by the modulator. The OSNR is intentionally degraded by adding amplified spontaneous emission (ASE) as additive white Gaussian noise (AWGN).

The degraded optical signal is received by the Rx front-end, comprising integrated dual polarised intradyne coherent receivers. The ADC converts the analogue input signals into quantised digital signals. After passing through the equaliser (EQ), the analogue signal is 3-bit quantised for SD based LDPC decoding. The LDPC decoder decodes iteratively using the variable offset belief propagation algorithm. After LDPC decoding, the UEP-BCH decoder cleans up the residual error floor. The OTU4 de-framer extracts the original 103.125 Gb/s bit stream, and any bit errors are detected by the PRBS checker.

Fig. 3 shows the calculated and measured post-FEC BER as a function of pre-FEC Q. The solid curve is the error-correction performance of the triple-concatenated FEC calculated by Monte Carlo simulation. The filled circles show the measured values.

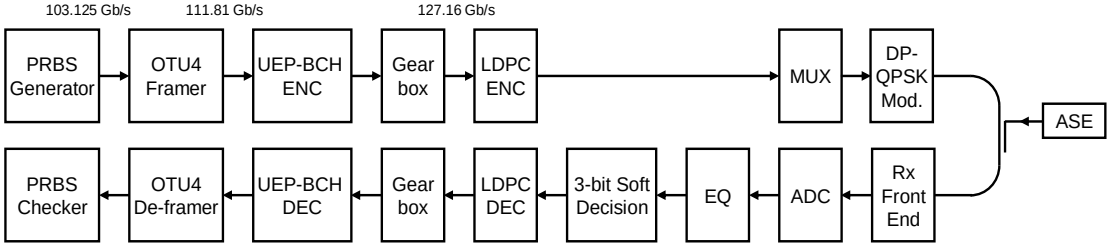

Figure 2: Experimental setup for triple-concatenated FEC performance.

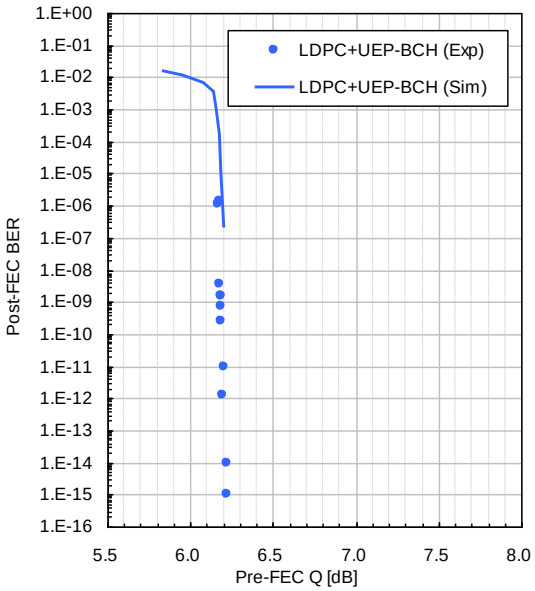

Figure 3: Experimental results for triple-concatenated FEC.

The calculated curve and the measured values agree well. We observed zero errors over 1 x 10^{15} bit counts at a post-FEC Q of 6.22 dB. The gross coding gain at an output BER of 1 x 10^{-15} is 11.7 dB. Taking the increased bit rate into account, the NCG is calculated to be 11.0 dB at this output BER. The NCG obtained is 1.7 dB away from the soft-decision Shannon limit for a binary input AWGN channel with 20.5% redundancy.

3 QUEST FOR MORE POWERFUL FEC

In order to meet the demands for transmission over transoceanic distances, binary phase shift keying (BPSK) is the best candidate because of its large Euclidean distance between adjacent symbols. However, this is not in itself a complete solution for transoceanic transmission, and combining it with more powerful FEC is essential. In this context, we propose a novel SD-FEC employing a spatially-coupled type irregular LDPC code which offers high performance in both the waterfall and error-floor regions [7].

It is known that an LDPC convolutional code offers high performance [8]. A spatially-coupled LDPC code, which is a super-class of the LDPC convolutional codes, also shows good performance [9]. In order to avoid the short cycles generated by the coupling of sub-matrices, we permute the rows of sub-matrices with columns of weight at least 3, and combine these with sub-matrices with columns of weight 2.

The LDPC code is constructed by adding a high column-weight sub-matrix to the coupling sub-matrix proposed above in accordance with the optimal distribution of column weights, in order to obtain higher performance. The code length is 38,400 bits and the number of parity bits is 7,568. Hence this LDPC(38400, 30832) code has 24.5% overhead. When concatenated with BCH(30832, 30592) with 0.78% redundancy, which can correct 16-bit errors, the total FEC redundancy is 25.5%.

The code length and the information bits of this concatenated code (38400, 30592) fit into an OTU4V frame. Note that all the columns of weight 2 in the parity-check matrix are assigned to the parity bits of the LDPC code.

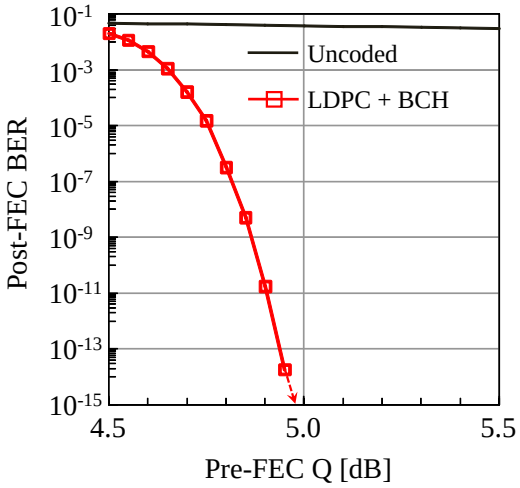

Figure 4: Simulation results for spatially-coupled type LDPC code.

The error correction performance of the proposed concatenation of LDPC(38400, 30832) and BCH(30832, 30592) codes was evaluated by Monte Carlo simulation in an additive white Gaussian noise (AWGN) channel. We used a simplified δ-min algorithm for the LDPC decoder, with 4 soft-decision bits. The number of iterations was set to 32. A δ-min algorithm is an approximation of belief propagation. Its error-correction performance is excellent, and hence the simplified version of the δ-min algorithm has better performance than the min-sum algorithm and its variants. The simulation results for post-FEC BER as a function of pre-FEC Q are shown in Fig. 4. We see no error-floor. The results indicate an NCG of 12.0 dB at a BER of 10^{-15}.

4 FUTURE PERSPECTIVE

The continuing evolution of the correction capacity of SD-FEC has pushed it to just 0.9 dB below the Shannon limit for a binary input AWGN channel with 25.5% redundancy. We can no longer expect the system performance to be improved by conventional means. Dealing with such issues as nonlinear effects in next-generation optical fibres and interference due to multi-dimensional multiplexing or modulation formats is a key issue for future optical transmission systems.

One approach to the further improvement of correction capability is turbo equalisation. Fig. 5 depicts the receiver structure for turbo equalisation pioneered by Douillard et al. [10]. By exchanging the extrinsic information between the decoder and the equaliser, it has been shown that iterating the equalisation and decoding tasks can yield tremendous improvements in the correction capability.

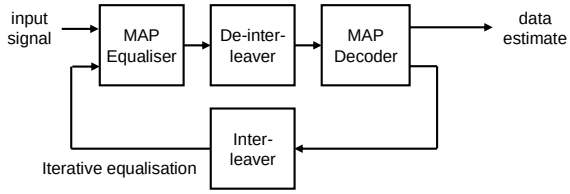

Figure 5: Combination of Turbo equalisation and SD-FEC.

Turbo equalisation has already been applied in practical wireless communication systems. However, in optical communications, this technology has not been applied commercially to date, due to the need for tremendously complex circuitry. Recently, the shrinking of CMOS devices has accelerated very aggressively in both research and production, and 22-nm gate length CMOS LSIs have now reached the point of practical use. Next-generation CMOS, with 16-nm gates, will enable us to combine SD-FEC and Turbo equalisation, resulting in more powerful system performance.

5 CONCLUSIONS

We have demonstrated the real-time performance of a triple-concatenated FEC with a 3-bit soft-decision LDPC code embedded in a coherent DSP and UEP-BCH codes embedded in an OTN framer. A Q-limit of 6.22 dB and an NCG of 11.0 dB at an output BER of 1×10^{-15} were obtained at 100 Gb/s. In addition, as a next generation FEC, we proposed the concatenation of a spatially-coupled type irregular LDPC with BCH codes. Numerical simulations indicated an NCG of 12.0 dB at a BER of 10^{-15}. For future capacity increases, nonlinearity equalisation is indispensable, the Turbo equaliser being a key enabler. It is anticipated that this new FEC and Turbo equaliser will drive increased capacity of future submarine cable systems at 100 Gb/s and beyond.

ACKNOWLEDGMENTS

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