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Enabling Global Communications

DQPSK Modulated Turbo Code FEC for Cable Capacity Upgrades

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Outline

- Introduction
  - Requirements for capacity upgrades
- Enabling technologies for capacity upgrades
- Challenges in implementing enabling technologies
  - DQPSK precoding technology
  - Soft decision Block Turbo Code FEC
- Experiment and Discussion
- Conclusion

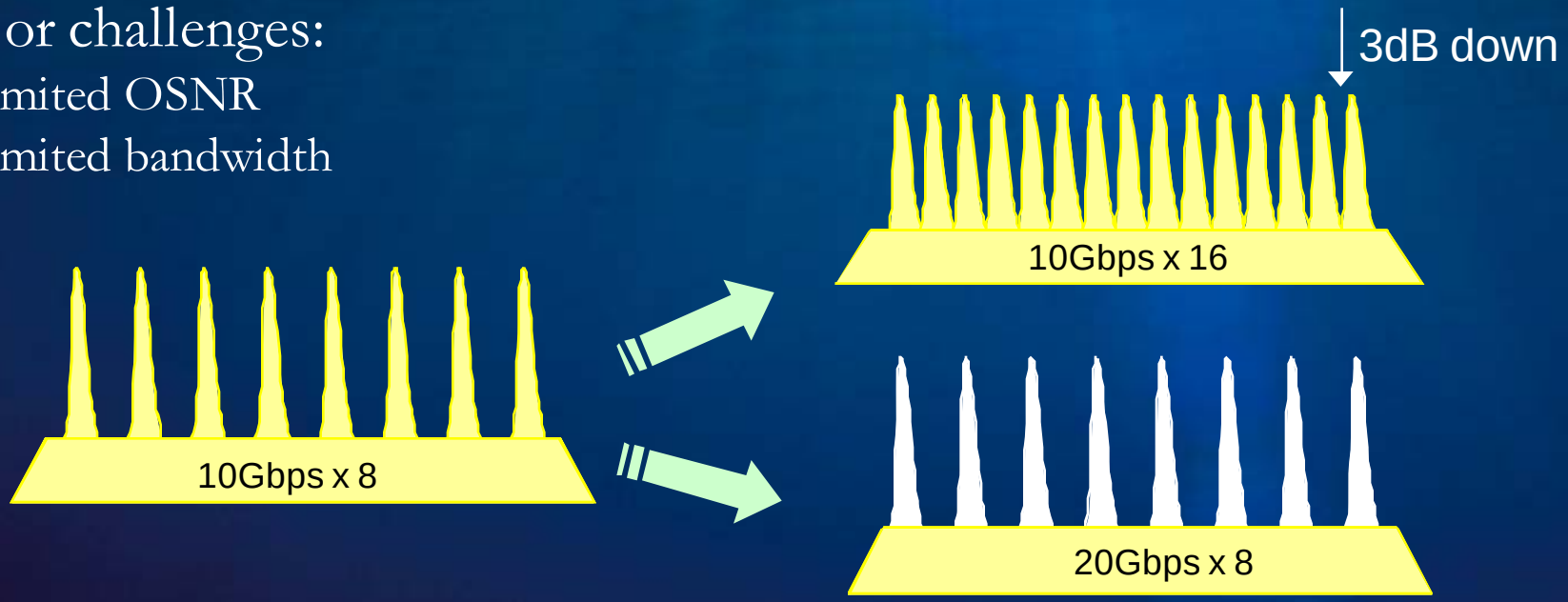
Requirements for upgrade

Capacity upgrade of existing submarine infrastructure:

- Increase the number of wavelengths
- Increase the bit-rate per wavelength

Major challenges:

- Limited OSNR
- Limited bandwidth

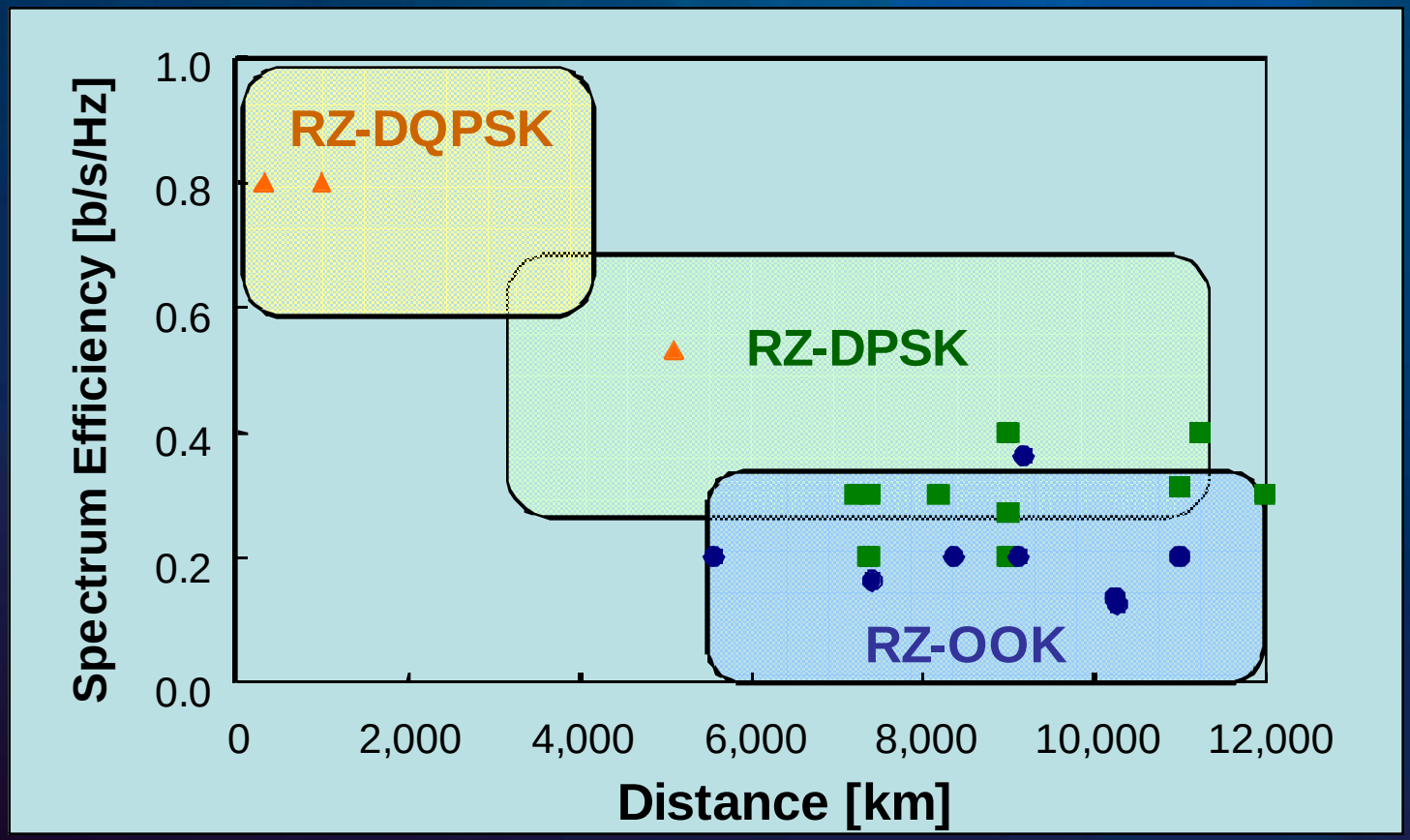


High sensitivity, spectrally efficient modulation format and strong FEC will be needed

Advanced Modulation Formats

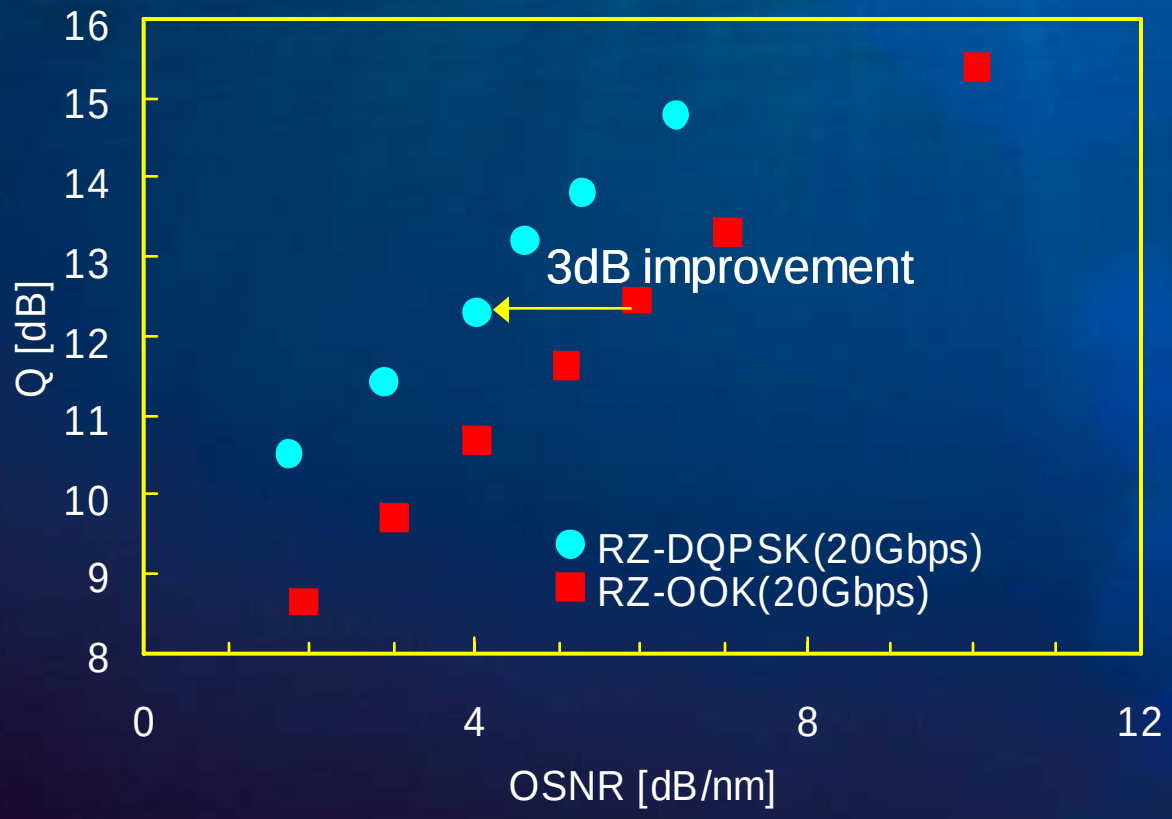
RZ-DQPSK seems ideal for short haul DWDM systems

- High spectral efficiency
- High sensitivity
- Acceptable nonlinearity tolerance



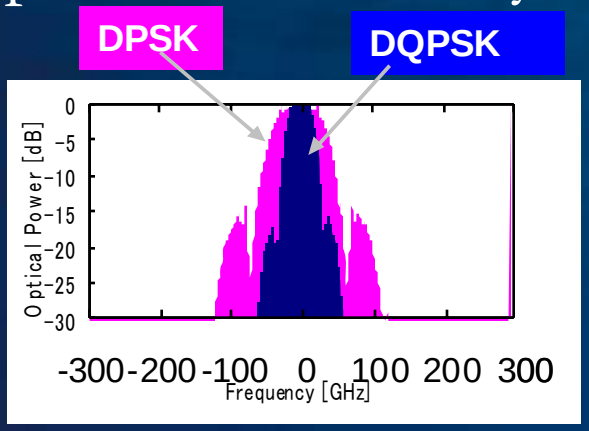
DQPSK: large tolerance to low OSNR

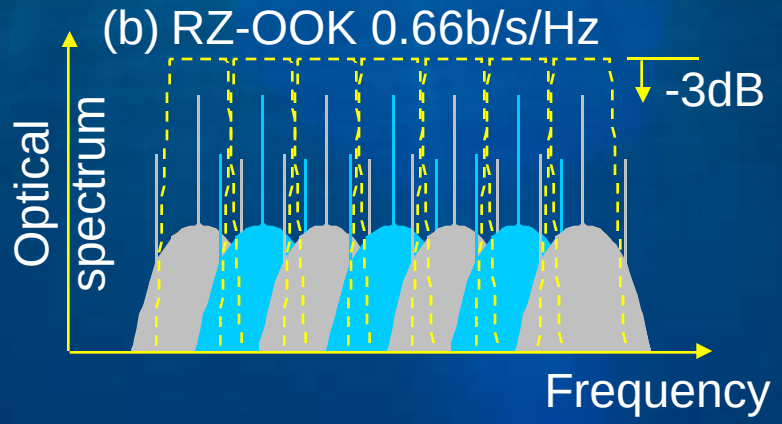
Phase Modulation & Balanced Detection improve tolerance to low OSNR by 3dB.



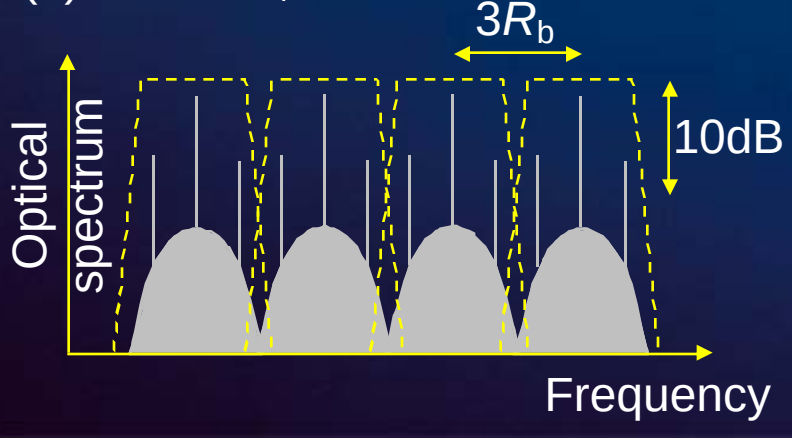
DQPSK: compact spectrum

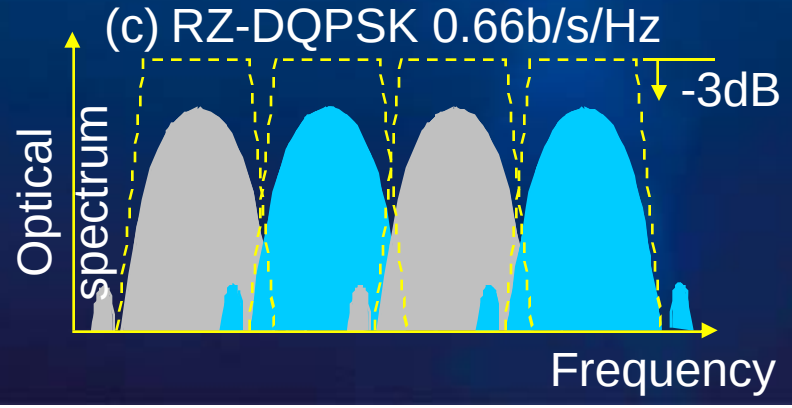
M-ary modulation formats such as DQPSK increase spectrum efficiency.





(a) RZ-OOK, 0.33b/s/Hz

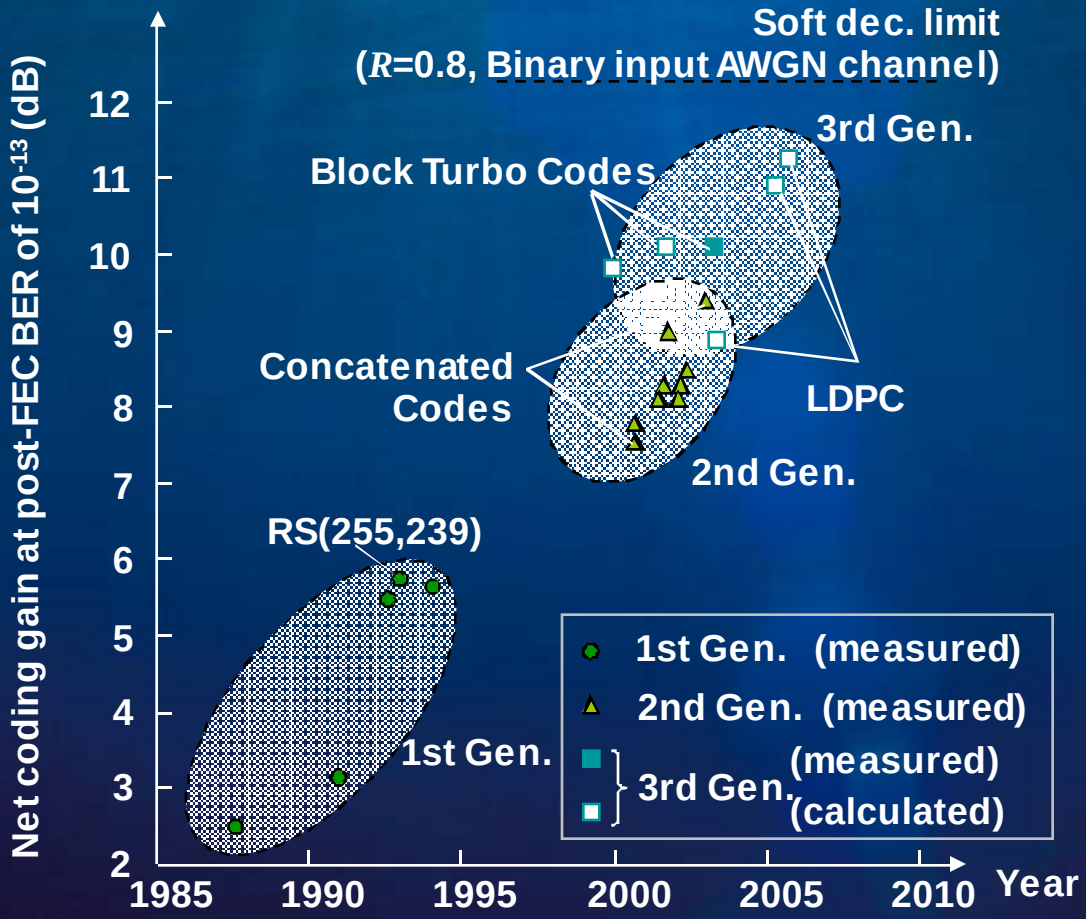




Strong FEC

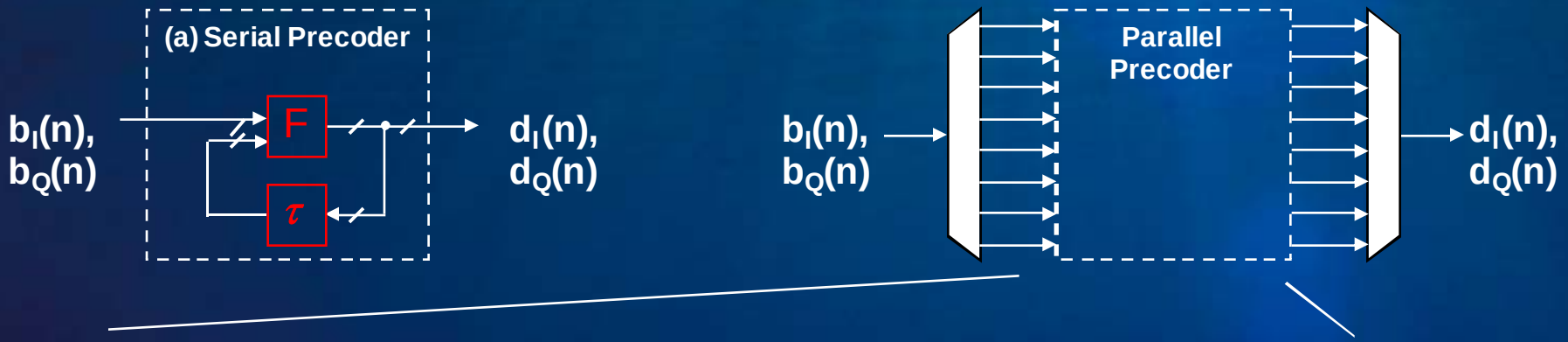
FEC has played an important role in optical communication systems.

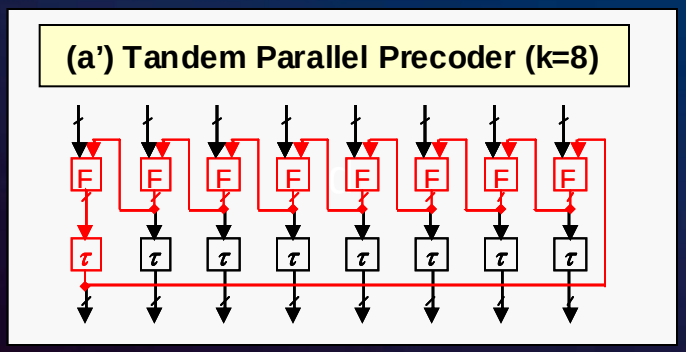
- 1st Gen.
  - 1988-1993
  - Hard decision
  - RS(255,239)
- 2nd Gen.
  - 2000~
  - Hard decision
  - Concatenated code
  - Best NCG of 9.4dB
- 3rd Gen.
  - Soft decision
  - Turbo code, LDPC
- Clear trend
  - NCG improvement of 1dB every 2 years



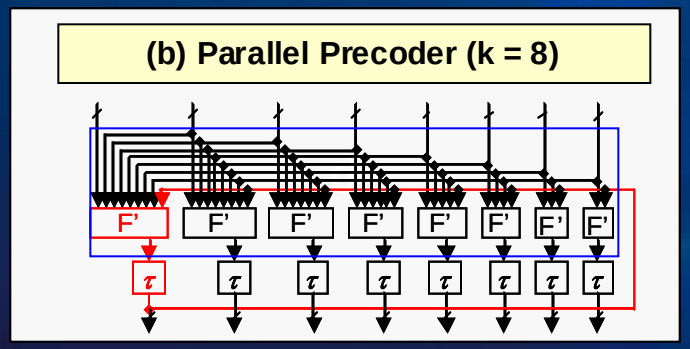
Challenges: DQPSK precoder

Challenges remain in implementation of large scale circuits: FEC coder/decoder and DQPSK precoding.





Circuit size: O(k) **Feed back path: O(k)**

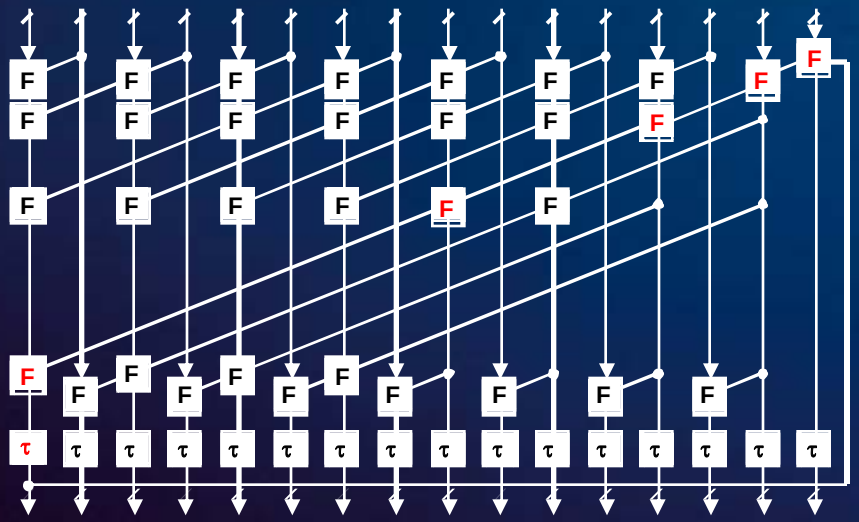


Circuit size: $O(k^2)$ Feed back path: $O(\log_2 k)$

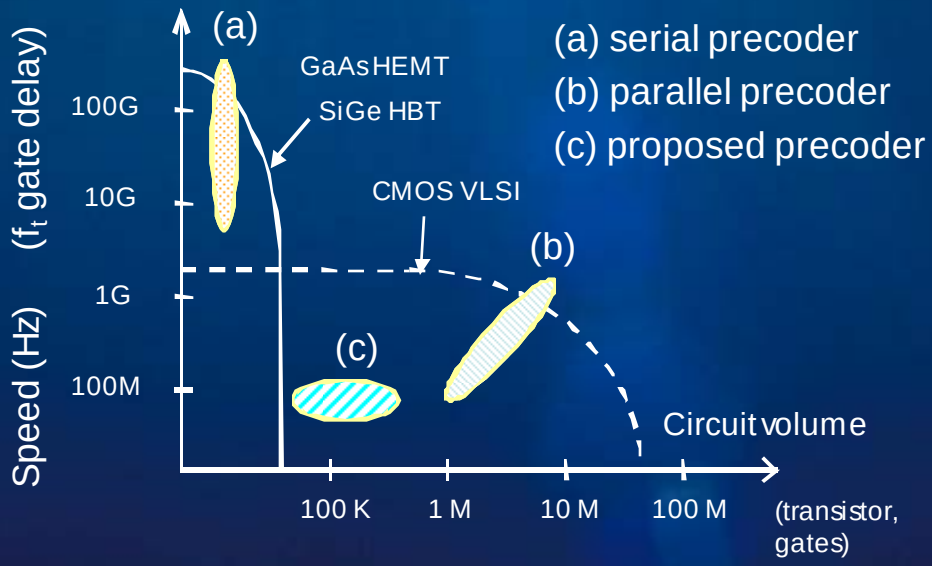
Challenges: DQPSK precoder

Proposed configuration makes it possible to reduce the circuit size and the required clock speed .

Proposed precoder based on Parallel prefix network



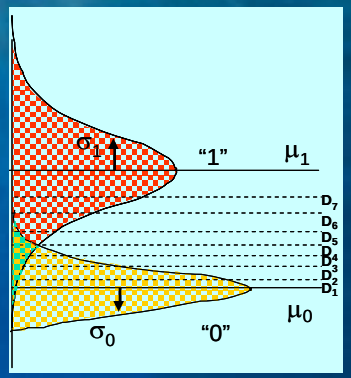
Comparison of DQPSK precoders

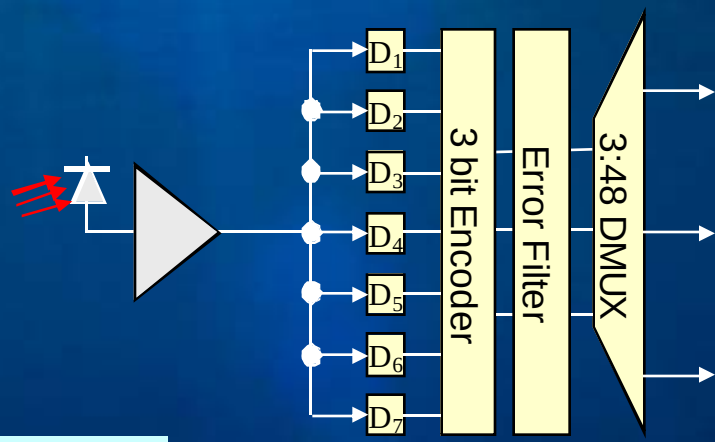


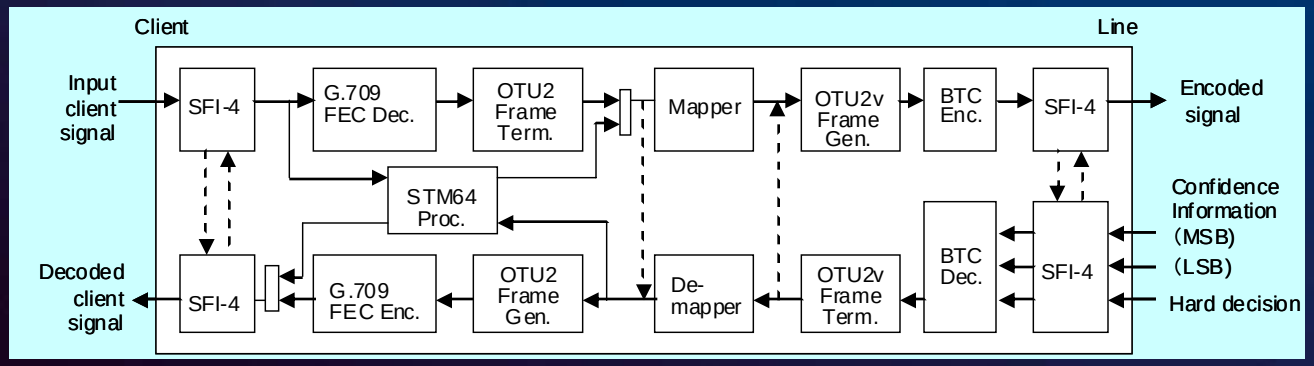
Challenges: FEC LSI

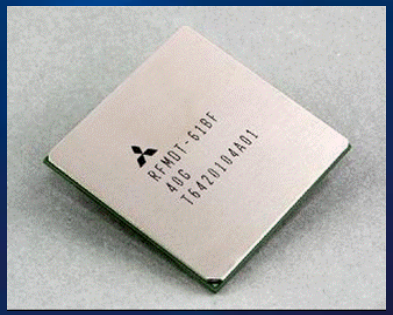
Soft decision and block turbo coding.

Throughput	10 Gb/s
Circuit size	16M Gates + 4Mbit RAM
Process	0.13μm CMOS
Package	1024-pin BGA, 1mm-pitch 40mm x 40mm
I/O	800Mb/s LVDS, SFI-4 I/F
Power supply	Core: 1.2V I/O: 2.5V, 3.3V
Power consumption	10W
Temp.	0~70 degrees C





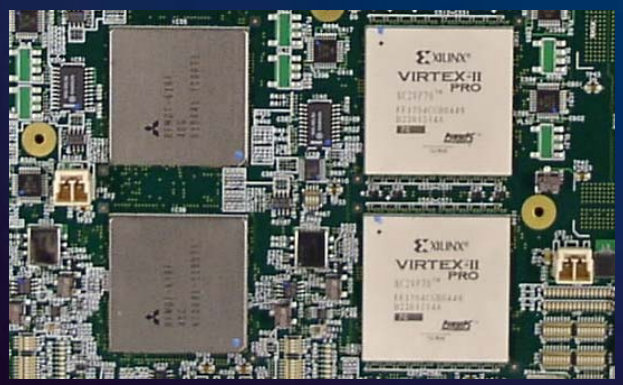




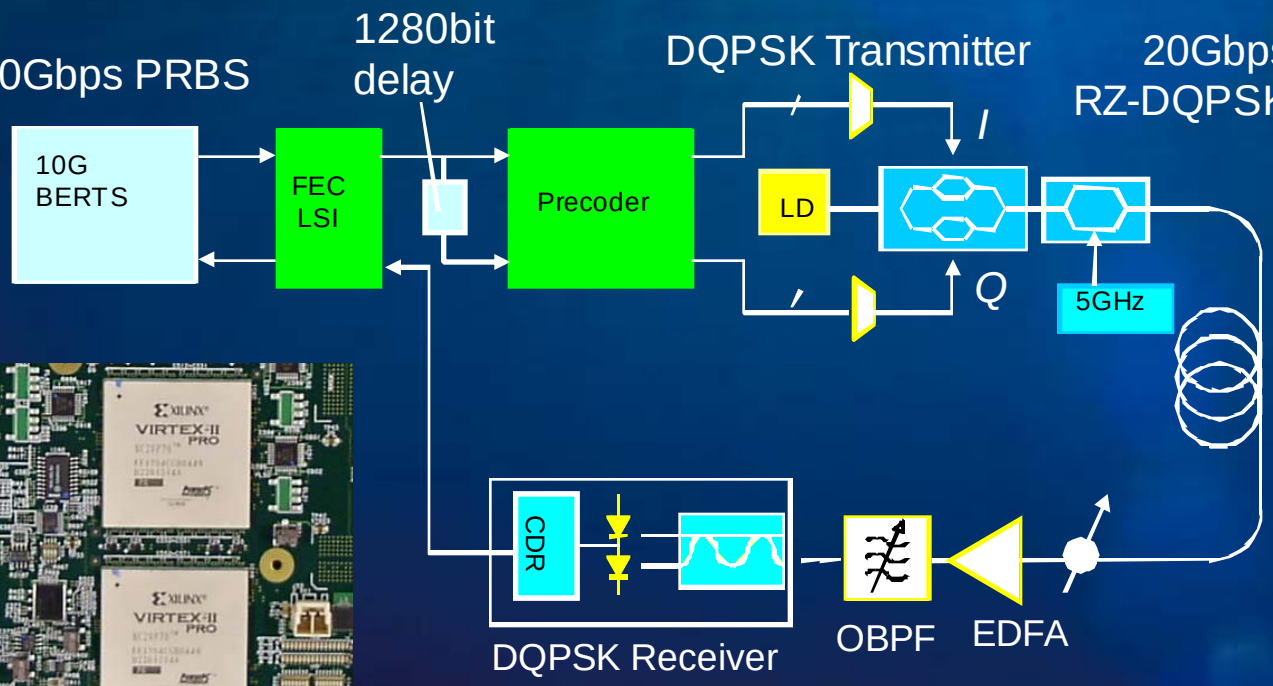
Experimental setup

BTC FEC LSI + parallel prefix decoder on one board.

20 Gbps DQPSK, PRBS 31, 23.6% redundancy



2x BTC FECs Precoder FPGA

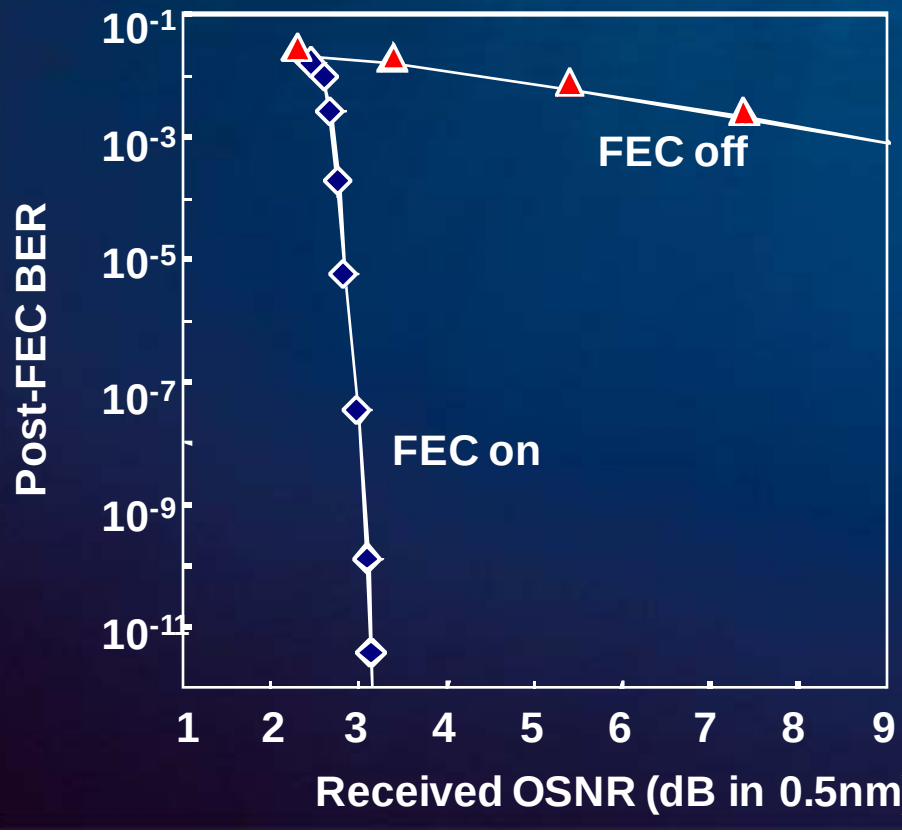


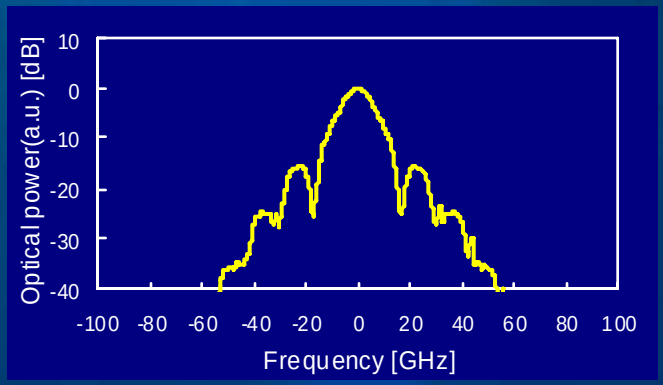
Measured data

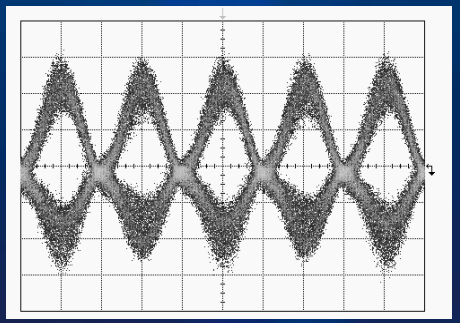
Measured FEC performance for 20Gbps DQPSK:

OSNR of 3.1 dB in 0.5 nm → BER = 3×10^{-12}

Net coding gain = 10.1 dB at BER of 1×10^{-13}

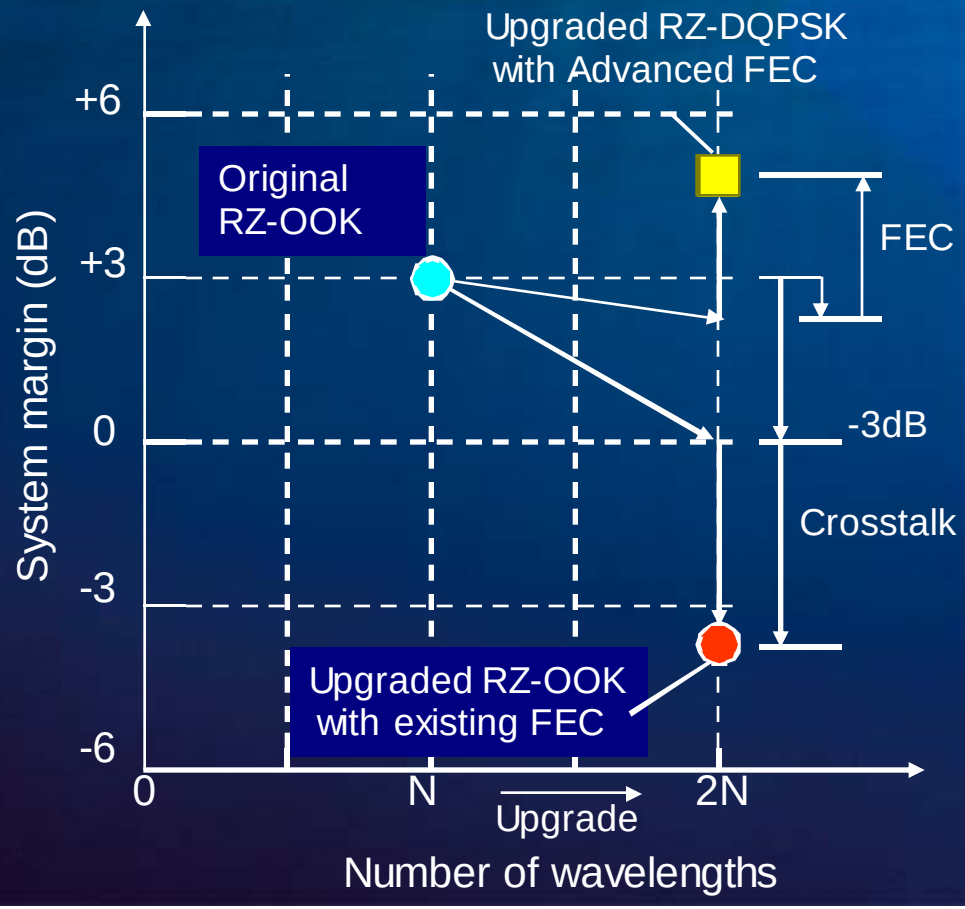






Upgrade with Strong FEC + DQPSK

The combination of strong FEC and DQPSK enables capacity upgrading with acceptable margins.



Conclusion

- DQPSK with its novel precoder provides a narrow spectrum with 3dB sensitivity improvement.
- The block turbo code FEC LSI provides a net coding gain of 10.1 dB.
- The combination of DQPSK and the strong FEC facilitates robust capacity upgrades of existing systems.

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